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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/777,694	02/07/2001	Kazutami Arimoto	49657-994	4365

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McDERMOTT, WILL & EMERY
600 13th Street, N. W.
Washington, DC 20005-3096

EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,694	ARIMOTO ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-12* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

   Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

   Information Disclosure Statement (IDS) filed on 2/7/01 was considered.

2. Claims 1-17 are presented for examination.

3. Claims 13-17 are withdrawn from consideration because they are included in the non-elected group of claims (see paper # 6).

4. Claims 1-12 are pending.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 1-4, and 8-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Taguchi et al, Pat. No. 6438055.

With regard to claim 1, Taguchi discloses a semiconductor memory device comprising: a memory array including plurality of memory cells arranged in a matrix (fig. 3, BLK); a refresh timer circuit (fig. 3, 21) providing a refresh request signal (fig. 3, REF1) at a time interval required to refresh data held by said plurality of memory cells; a command generation circuit (fig. 3, 12 and 24) generating an internal command signal (fig. 3, CMD1, RD, WR) according to an access command (fig. 3, CMD); and a row selection control circuit (fig. 3, 28)) carrying out an operation associated with row selection of said memory array according to said internal command signal (fig. CMD1 to RD and WR to SEL) and said refresh request signal (fig. REF1 to REF to SEL), said row selection control circuit including a timing control circuit (fig. 3, CLK1 received by 24) rendered active according to said internal command signal (fig. 3, CMD1) to output timing signals (col. 7, line 60 – col. 8, line 5) of a row selection operation of said memory array, a refresh control circuit (fig. 3, 25) receiving and holding said refresh request signal (fig. 3, REF1) to output an internal refresh command signal (fig. 3, REF) when said timing control circuit attains an inactive state, and a refresh timing control circuit (fig. 3, 26) rendered active according to said internal refresh command signal (fig. 3, REF) to output said timing signal instead of said timing control circuit; and a row selection circuit (fig. 3, 28) carrying out row selection of said memory array according to said timing signal (col. 7, line 60 – col. 8, line 5).

With regard to claim 2, Taguchi discloses wherein said access command includes a read command (col. 3, line 51-55), wherein a basic cycle time of said semiconductor memory device starting from reception of said access command up to attaining a state that allows reception of the next access command is at least a total time of a normal read cycle time starting from output of said internal command signal up to completion of data read out from said memory array and a refresh cycle time starting from output of said internal refresh command signal up to completion of refresh of a portion in said memory array corresponding to said internal refresh command signal (col. 7, line 60 – col. 9, line 52).

With regard to claim 3, Taguchi discloses wherein the refresh control circuit (fig. 3, element 25 or fig. 5) comprises a latch circuit (fig. 5, 37) receiving and holding the refresh request signal (fig. 5, REF1 to RFL to N1), a pulse generation circuit (fig. 5, 38) providing a pulse that becomes a basis of the internal command signal when an output of the latch circuit indicates input of the refresh request signal and the timing control circuit is at an inactive state (col. 9, line 12-52).

With regard to claim 4, Taguchi discloses the command generation circuit holds the access command, and waits for inactivation of said refresh timing control circuit to output the internal command signal when the refresh timing control circuit is active (col. 7, line 60 - col. 8, line 5).

With regard to claim 8, Taguchi discloses a data input/output control circuit (fig. 3, 16) receiving and holding as read out data an output from said memory array, and receiving an output enable signal (fig. 3, I/ODB) to output said read out data.

With regard to claim 9, Taguchi disclosed wherein row selection control circuit further comprises: an address latch circuit holding (fig. 3, 14) an applied row address (fig. 3, A0-An) to output a normal row address (fig. 3, EAdd), a refresh counter circuit (fig. 3, 22) sequentially updating and providing a refresh row address (fig. 3, RAdd) corresponding to a row to be refreshed, and a select circuit (fig. 3, 28) receiving the normal row address (fig. 3, EAdd) and the refresh row address (fig. 3, RAdd) to output one of the normal row address and the refresh row address as an address corresponding to row selection of the memory array according to the internal refresh command signal.

With regard to claim 10, Taguchi disclosed the memory array includes a plurality of banks (fig. 3, Bank0, Bank1) that allows a row select operation independently, wherein the refresh control circuit outputs the internal refresh command signal after the refresh control circuit attains an inactive state when a bank indicated by the normal row address coincides with a bank indicated by the refresh row address (col. 1, line 24-64).

With regard to claim 11, Taguchi discloses wherein the address latch circuit accepts the applied row address in synchronization with a clock signal (fig. 3, 14 received A0-An and CLK1).

With regard to claim 12, Taguchi discloses a latch circuit (fig. 3, 24) accepting the access command (fig. 3, CMD1) in synchronization with a clock signal (fig. 3, CLK1, CKE) and providing the access command to the command generation circuit (fig. 3, RD, WR).

Allowable Subject Matter

6. Claim 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of said control circuit includes the command generation circuit comprises: an internal command generation circuit providing a command generation reference signal according to the access command, and a delay circuit delaying the command generation reference signal for at least the refresh cycle time and providing the internal command signal, wherein the refresh control circuit receives and holds the refresh request signal to output the internal refresh command signal when the timing control circuit attains an inactive state.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Jang (6219292) and Schaefer (5600605) disclose a memory device.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

January 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818